IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	Atty. Docket
ALEXANDER PADIY ET AL.	FR 030037
	Confirmation No. 6182
Serial No. 10/552,059	Group Art Unit: 2627
Filed: OCTOBER 4, 2005	Examiner: NWAKAMMA, C.K.

Title: CROSS-TALK CANCELLATION SCHEME FOR RLL-BASED STORAGE SYSTEMS

Mail Stop Appeal Brief-Patents
Board of Patent Appeals and Interferences
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

Appellants herewith respectfully present a Brief on Appeal as follows, having filed a Notice of Appeal on September 25, 2008:

REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee of record Koninklijke Philips Electronics N.V., a corporation of The Netherlands having an office and a place of business at Groenewoudseweg 1, Eindhoven, Netherlands 5621 BA.

RELATED APPEALS AND INTERFERENCES

Appellants and the undersigned attorney are not aware of any other appeals or interferences which will directly affect or be directly affected by or having a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1 and 3-8 are pending in this application, where claim 2 had been canceled by an Amendment filed on August 25, 2008 in response to a Final mailed on June 25, 2008. Claims 1 and 3-8 are rejected in the Final Office Action mailed in June 25, 2008. This rejection was upheld, in the Advisory Action that was mailed on September 12, 2008. Claims 1 and 3-8 are the subject of this appeal.

STATUS OF AMENDMENTS

Appellants filed on August 25, 2008 an after final amendment in response to a Final Office Action mailed June 25, 2008. The after final amendment includes a minor amendment to claim 1 and canceled claim 2. In an Advisory Action mailed on September 12, 2008, it is not indicated whether the Amendment filed on August 25, 2008 is entered. It is assumed that this August 25, 2008 Amendment is entered as it corrects the specification as per the Examiner's suggestions, and cancels claim 2, thus rendering moot a rejection thereto and simplifying issues on appeal. The Advisory Action mailed on September 12, 2008, further indicates that the after final amendment filed on August 25, 2008 does not place the application in condition for allowance. This Appeal Brief is in response to the Final Office Action mailed June 25, 2008, that finally rejected claims 1 and 3-8, which remain finally rejected in the Advisory Action mailed on September 12, 2008.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The present invention, for example, as recited in independent claim 1, is directed to a cross-talk cancellation method using a main signal 62 associated with a target track 31 and satellite signals 61, 63 associated with side tracks 31, 33, shown in FIGs 3-5, and described on page 5, lines 1-7 and page 5, lines 17-30. The main signal has transitions X_m and runs of various lengths $d_{m+1,m}$ between two transitions X_m, X_{m+1}, as shown in FIG 6, and described on page 6, line 18 to page 8, line 7.

As shown in FIGs 3-5, and described on page 5, lines 17-30, the cancellation method comprises the acts of sampling the satellite signals 61, 63 to form sampled satellite signals with converters 51, 53 that receive a fixed clock 551 and filtering the satellite signals with adaptive filters 71, 73 that run on the fixed clock 55, thereby generating filtered versions 81, 83 of the satellite signals 61, 63.

As shown in FIG 6, and described on page 6, lines 4-24, the method further includes updating coefficients of the adaptive

filters 71, 73 by minimizing a mismatch between an actual run length and an expected run length between the two transitions of the main signal 62; and processing the main signal 62, thereby generating an improved main signal 102.

As shown in FIG 5, and described on page 5, line 17 to page 6, line 3, the processing includes a subtraction of the filtered versions 81, 83 of the satellite signals from the main signal 62, 92; and providing the improved main signal 102 to a sample rate converter 102 driven by a bit clock 130. Further, as described on page 6, lines 1-7, and page 6, line 25 to page 7, line 15, the method also includes estimating a ratio between the bit clock and the fixed clock, and taking the ratio into account during the updating act.

The present invention, for example, as recited in independent claim 3, is directed to a signal processor 40 shown in FIG 1 and described on page 5, lines 12-16. The signal processor 40 comprises cross-talk cancellation means 42 for receiving a main signal 62 associated with a target track 32 and satellite signals 61, 63 associated with side tracks 31, 33, shown in FIGs 3-5, and

described on page 5, lines 1-7 and page 5, lines 17-30. The cross-talk cancellation means 42 is shown in greater detail in FIG 5 and described on page 5, lines 17-30, and includes converters 51-53 that receive the main and satellite signals 61-63.

The main signal has transitions X_m and runs of various lengths $d_{m+1,m}$ between two transitions X_m, X_{m+1}, as shown in FIG 6, and described on page 6, line 18 to page 8, line 7. As shown in FIGs 3-5, and described on page 5, lines 17-30, the cross-talk cancellation means 42 comprises filtering means, such as adaptive filters 71, 73 for filtering the satellite signals 61, 63, thereby generating filtered versions 81, 83 of the satellite signals.

As shown in FIGs 5-6, and described on page 6, lines 4-24, the cross-talk cancellation means 42 further includes updating means, such as updating devices 111, 113 for updating coefficients of the adaptive filters 71, 73 by minimizing a mismatch between an actual run length and an expected run length between the two transitions of the main signal. The cross-talk cancellation means 42 also includes processing means, such as a subtractor 93, for generating an improved main signal 102 from the main signal by subtraction of

said filtered versions of the satellite signals from the main signal 62, 92.

As described on page 6, lines 1-7, and page 6, line 25 to page 7, line 15, the cross-talk cancellation means 42 further includes time recovery means, such as a sample rate converter 120 driven by a bit clock 130 shown in FIG 5, for estimating a ratio between the bit clock 130 and a fixed clock 55 that drives the adaptive filters 71, 73, and for providing the ratio to the updating devices 111, 113 where the updating device 111 is designed to take the ratio into account for updating the coefficients of the adaptive filters 71, 73.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1 and 3-8 of U.S. Patent Application Serial No. 10/552,059 are unpatentable under 35 U.S.C. §103(a) over U.S. Patent Application Publication No. 2002/0034268 (Miyanabe) in view of U.S. Patent No. 6,134,211 (Miyanabe-211) and U.S. Patent No. 5,703,845 (Audoin).

ARGUMENT

Claims 1 and 3-8 are said to be unpatentable over Miyanabe in view of Miyanabe-211 and Audoin.

Appellants respectfully request the Board to address the patentability of independent claims 1 and 3, and further claims 4-8 as depending from independent claim 3, based on the requirements of independent claim 3. This position is provided for the specific and stated purpose of simplifying the current issues on appeal. However, Appellants herein specifically reserve the right to argue and address the patentability of claims 4-8 at a later date should the separately patentable subject matter of claims 4-8 later become an issue. Accordingly, this limitation of the subject matter presented for appeal herein, specifically limited to discussions of the patentability of independent claims 1 and 3 is not intended as a waiver of Appellants' right to argue the patentability of the further claims and claim elements at that later time.

On page 5, of the Final Office Action, the Examiner correctly

noted that Miyanabe does not disclose or suggest "sampling said satellite signals to form sampled satellite signals with converters that receive a fixed clock; [and] filtering said satellite signals with adaptive filters that run on a fixed clock," as recited in independent claim 1, and similarly recited in independent claim 3. Miyanabe-211 is cited in an attempt to remedy the deficiencies in Miyanabe.

Miyanabe-211 shows in FIGs 1 and 5 converters 5a-5c that receive a clock from a PLL circuit 10. As specifically recited on column 1, lines 42-47 and column 5, lines 62-67, the PLL circuit 10 "generates a clock signal having an oscillating frequency corresponding to the amount of a phase error, and supplies the clock signal to the A/D converters 5a-5c." (Column 1, lines 46) That is, the clock signal frequency is not fixed and depends on the amount of error. This is even acknowledged in the Final Office Action, page 5, third full paragraph, where the PLL generated clock is analogized to the bit clock. Accordingly, Miyanabe, Miyanabe-211, and combination thereof do not disclose or suggest "sampling said satellite signals to form sampled satellite signals with

converters that receive a fixed clock; [and] filtering said satellite signals with adaptive filters that run on the fixed clock," as recited in independent claim 1, and similarly recited in independent claim 3. (Illustrative emphasis provided)

Assuming, arguendo, that the combination of Miyanabe and Miyanabe-211 disclose or suggest that above noted features of the present application, Miyanabe and Miyanabe-211 still do not disclose or suggest "estimating a ratio between the bit clock and the fixed clock, and taking said ratio into account during the updating act," as recited in independent claim 1, and similarly recited in independent claim 3, and as correctly noted on page 6 of the Final Office Action. Element 4 in FIGs 7a-b and 10a, and column 6, lines 11-15 of Audoin are cited in an attempt to remedy the deficiencies Miyanabe and Miyanabe-211.

It is respectfully submitted that the noted sections of Audoin merely disclose signals such as Cgp Cdp, Cgi, Cdi, Egp and Edp. Each of these signals is not representative of any ratio. It is alleged that Egp and Edp represent ratios, but column 5, lines 65-66 specifically recite that Egp and Edp are two elements multiplied

together, namely:

Edp=X'p(k-1) * Sgn[X'i(k-1)] and

Egp=X'p(k-1) * Sgn[X'i(k-2)]

There is simply no disclosure or suggestion in Miyanabe, Miyanabe-211, and Audoin, alone or in combinations, of any ratio, let alone teaching or suggesting "a ratio between a bit clock that drives the time recovery means and a fixed clock that drives the filtering means, and ... providing said ratio to said updating means," as recited in independent claim 3, and similarly and recited in independent claim 1.

The last 4 lines of the Advisory Action alleges that it is admitted, on page 7, lines 3-8 of the present application, to be well known to provide to updating means a ratio between a bit clock that drives the time recovery means and a fixed clock that drives a filtering.

Appellants strongly disagree and point out that page 7, lines 3-8 of the present application merely recite that an external time recovery circuit is already present in conventional reading devices and that a ratio may be estimated using circuits present in

conventional reading devices. This in no way discloses or suggests that conventional devices using any ratio or provide any ratio to any updating means," as recited in independent claim 3, and similarly and recited in independent claim 1. Rather, page 7, lines 3-8 of the present application point out that a ratio may be generated and provided to updating means with minimal changes or additions to conventional reading devices, resulting in a relatively inexpensive implementation of the present invention.

In view of the foregoing, it is respectfully submitted that independent claims 1 and 3 should be allowable, and allowance thereof is respectfully requested. In addition, it is respectfully submitted that claims 4-8 should also be allowed at least based on their dependence from amended independent claim 1.

In addition, Appellants deny any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, the Appellants reserve the right to submit further arguments in support of the above stated position,

should that become necessary. No arguments are waived and none of the Examiner's statements are conceded.

CONCLUSION

Claims 1 and 3-8 are patentable over Miyanabe in view of Miyanabe-211 and Audoin.

Thus, the Examiner's rejections of claims 1 and 3-8 should be reversed.

Respectfully submitted,

By _____
Dicran Halajian, Reg. 39,703
Attorney for Appellants
November 24, 2008

THORNE & HALAJIAN, LLP
Applied Technology Center
111 West Main Street
Bay Shore, NY 11706
Tel: (631) 665-5139
Fax: (631) 665-5101

CLAIMS APPENDIX

1.(Previously Presented) A cross-talk cancellation method using a main signal associated with a target track and satellite signals associated with side tracks, said main signal showing transitions and runs of various lengths between two transitions, said cancellation method comprising the acts of:

sampling said satellite signals to form sampled satellite signals with converters that receive a fixed clock;

filtering said satellite signals with adaptive filters that run on the fixed clock, thereby generating filtered versions of said satellite signals,

updating coefficients of said adaptive filters by minimizing a mismatch between an actual run length and an expected run length between the two transitions of the main signal,

processing said main signal, thereby generating an improved main signal, said processing including a subtraction of said filtered versions of said satellite signals from the main signal,

providing the improved main signal to a sample rate converter driven by a bit clock,

estimating a ratio between the bit clock and the fixed clock, and

taking said ratio into account during the updating act.

Claim 2 (Canceled)

3.(Previously Presented) A signal processor comprising cross-talk cancellation means for receiving a main signal associated with a target track and satellite signals associated with side tracks, said main signal showing transitions and runs of various lengths between two transitions, said cross-talk cancellation means comprising:

filtering means for filtering said satellite signals with adaptive filters, thereby generating filtered versions of said satellite signals,

updating means for updating coefficients of said adaptive filters by minimizing a mismatch between an actual run length and

an expected run length between the two transitions of the main signal,

processing means for generating an improved main signal from said main signal by subtraction of said filtered versions of the satellite signals from the main signal,

time recovery means for estimating a ratio between a bit clock that drives the time recovery means and a fixed clock that drives the filtering means, and for providing said ratio to said updating means, said updating means being designed to take said ratio into account for updating said coefficients.

4.(Previously Presented) The signal processor as claimed in claim 3, wherein said fixed clock is asynchronous with respect to said bit clock, and wherein said cross-talk cancellation means are operated at said fixed clock.

5.(Previously Presented) The signal processor as claimed in claim 4, wherein said bit clock has a bit clock frequency and said fixed clock has a fixed clock frequency that is substantially

different from said bit clock frequency such that the ratio between said bit clock frequency and said fixed clock frequency is substantially different from one.

6.(Previously Presented) An apparatus for reading a signal stored along a track on a storage medium comprising a signal processor as claimed in claim 3.

7.(Original) An apparatus for reading a signal stored along a track on a storage medium comprising a signal processor as claimed in claim 4.

8.(Original) An apparatus for reading a signal stored along a track on a storage medium comprising a signal processor as claimed in claim 5.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None